

The SPIRIT Consortium

IP-XACT 1.4

ESL Extensions

IP-SoC 2006

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The
SPIRIT
Consortium



ESL Working Group (EWG)

- **Contributing Member Companies:**
 - ARM, Cadence, CoWare, Infineon, LSI Logic, Mentor Graphics, NXP Semiconductors, ST Microelectronics, Synopsys
- **Goals:**
 - Only standardize on existing standards or de-facto standard industry proven modeling methodologies that can apply to all standard HW languages
- **Scope:**
 - Restrict ESL scope to Transactional Level Modeling (TLM) of IP and platforms
 - Support current TLM Design and Verification methodologies

ESL Working Group (EWG)

– Charter:

- Enhance IP-XACT version 1.2 to support
 - TLM IP modeling (support SC, SV...)
 - Design IP, Verification IP
 - TLM System Design modeling
 - Mix TLM-RTL designs, mix Transactional levels

– Deliveries:

- 1.4 schema additions
- Documentation (User Guide, Application notes)
- Examples (TLM and mix TLM-RTL designs)
- Semantic rules checker additions

TLM problems: SystemC IP

- **Represent Ports**
 - Describe `sc_port`, `sc_export`
 - Describe `sc_interface`
 - Port access: by reference, by pointer
 - Port handle: by name, by function
- **Represent Parameters**
 - Module (class) constructor and template parameters
 - Pre-processor directives (`#ifdef`, macros)
- **Represent abstraction levels**
 - Convert/refine from one abstraction level to another
 - Not standardized (yet ☹)
- **Represent implementation files**
 - Source files, Include files

TLM problems: SystemVerilog IP

- **Represent New data types**
 - Class, union, struct...
- **Represent SV Interfaces**
 - cannot be mapped to a busDefinition because
 - modPort not restricted to master, slave, system
 - missing mapping of modPort to Component ports
 - Represented as a complex port in Component
 - Port access: modPort
 - Port handle: function, task
- **Represent Parameters:**
 - Module and Interface type and non-type parameters
- **Represent implementation files**
 - Source files, include files

TLM problems: mix TLM and RTL

- **Represent Mix abstraction level designs**
 - E.g. RTL DUT and TLM verification components
 - E.g. Progressive refinements of an IP
- **Connect components with bus interfaces at different levels of abstraction**
 - Represent interface adapters (i.e. Abstractors)
 - Represent protocol adapters (i.e. Transactors)
 - Represent transaction recording (i.e. Monitors)

EWG proposed solution for IP-XACT 1.4

- **General concepts**
 - Each abstraction level model of an IP (e.g. OSCI TLM PV, PV, CA, RTL) is represented as different IP-XACT components
 - Related components can (only) be grouped by name (e.g. same Library name in VLNV)
 - Can have different ports, different interfaces, different memoryMap...
 - Extend the IP-XACT design connectivity semantic rule to allow connection between two components with different interfaces (i.e. different busDefinition)
 - The interconnection must define an abstractor capable of converting from one interface to the other

**Still under validation
(i.e. may change!)**

EWG proposed solution for IP-XACT 1.4

- **Represent Ports**
 - **Extend signal to support complex ports**
 - Port Type: wire or cable
 - Port Direction: direction (in, out, inout) for wire, (provide, require interface) for cable
 - Port Protocol: interface definition for cable
- **Represent Parameters:**
 - **Extend modelParameters to support:**
 - type (e.g template) parameters
 - User defined (e.g.Pre-processor directives) parameters
- **Represent implementation files:**
 - New fileTypes added, Include files supported

**Still under validation
(i.e. may change!)**

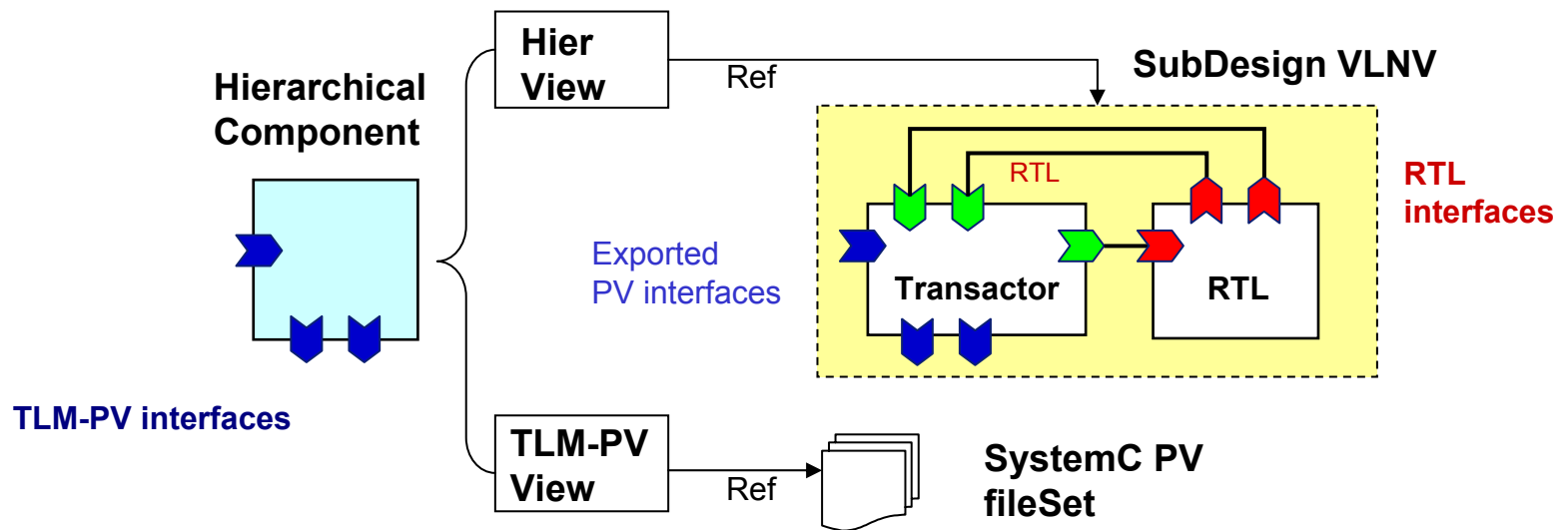
EWG proposed solution for IP-XACT 1.4

- **Represent Abstractors**
 - Bridge between different abstraction level interfaces
 - Unlike other components, do not go on Silicon
 - Represented as a specific schema object with 2 interfaces
- **Represent Monitors**
 - Observe traffic on a connection
 - RTL and TLM monitors can be very different
 - E.g. analysis interface on ports in OSCI TLM 2.0 kit
 - Separate module with connected ports at RTL
 - Represented as a specific schema object with passive interfaces

**Still under validation
(i.e. may change!)**

EWG proposed solution for IP-XACT 1.4

- Represent multiple abstractions of a IP
 - Reuse the 1.2 hierarchical component feature
 - Align on one abstraction level
 - E.g. one TLM-PV view and one hierarchical view



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(i.e. may change!)**

Already available

- **Previous deliveries:**
 - Jan 2006: 1.4 alpha (to reviewing members only)
 - July 2006: 1.4 alpha2 (to reviewing members only)
 - Dec 2006: 1.4 alpha3 (to reviewing members only)
- **Current activities:**
 - Validate 1.4 by developing IP and tools
 - Refine 1.4 schema and TGI specification as validation progresses
- **Future deliveries:**
 - Depend on validation progress on both tool and IP side

Want to see more and sooner?

- Willing to access early development versions of 1.4?
- Willing to help validate 1.4 on your IP ?
- Willing to accelerate the delivery of the 1.4 version?
- Willing to influence current or future versions?

Your feedback and contributions are more than welcome

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