

## Arteris and Duolog Streamline SOC Integration Design Flow

*Duolog chip integration platform provides system-level and software views of Arteris network-on-chip (NoC) architectures*

**SAN JOSE, Calif. – June 15, 2009 - Arteris Inc**, the leading developer of Network on Chip (NoC) solutions and **Duolog**, a provider of SoC integration tools, today announced the integration of Duolog design tools with Arteris' NoC solution to provide designers a more streamlined and efficient way to integrate multiple semiconductor intellectual property (IP) blocks on a single system on ship (SoC) device. The integration leverages Arteris' NoC solution for enabling high-performance on-chip interconnect and communications, and Duolog's Socrates™ Chip Integration Platform, which is a suite of tools for capturing, viewing and validating various elements of the infrastructure of complex SoCs.

The integration uses the industry standard IP-XACT format, a standard way to describe and handle IP from multiple sources. Using the Arteris NoCcompiler™ tool, SoC designers can quickly configure, instantiate, and connect NoC IP units to generate specific NoC instance(s), including full RTL and verification infrastructures. As part of this NoC IP instance generation, NoCcompiler generates an IP-XACT description which includes high-level interfaces, ports and memory map data.

The Duolog system uses the IP-XACT description to allow designers to capture the software view of the system from low-level IP registers and bitfields to the full system-level memory map. Its Socrates Bitwise™ register management tool not only captures the complete memory map infrastructure but provides real-time views from any point on the memory map. It generates a wide range of collateral including documentation, hardware design and verification infrastructures and software API models.

"With this integration, we have been able to add a new register to an IP to automatically generate a new software API and corresponding documentation at the chip level, all in less than a minute. For this level of turnaround time we need to ensure we clearly understand the NoC memory mapping, which is what our close collaboration with Arteris has allowed," said Ray Bulger, CEO of Duolog. "We have worked closely with Arteris and several of our customers to ensure that we align on the memory map content via the IP-XACT standard and have proved that this level of tool coupling can significantly improve the efficiency of streamlining our mutual customers' IP integration flow."

The streamlined flow also incorporates Duolog's Socrates Weaver™, a rules-based assembly engine that enables rapid and robust interface and port-level connectivity to ensure that the chip integration can happen sooner and more predictably.

"The integration of our NoC generation system with Duolog's viewing and validation capabilities provides a robust and efficient way to integrate complex SoCs," said Charlie Janac, CEO of Arteris "Our customers can use the Arteris NoC IP and tools to rapidly generate NoC instance IPs to very quickly achieve their system performance goals. By combining our NoC approach with Duolog's tools, customers can integrate the Arteris NoC Instance IPs with the rest of the SoC to produce earlier software and hardware deliveries. By using standards such as IP-XACT to package the NoC IPs, it is an extremely interoperable approach that allows the use of a wide a variety of IP."

The integrated Arteris/Duolog solution will be demonstrated at the **2009 Design Automation Conference in San Francisco (July 26-31) in the Duolog Booth #2028.**

**About Duolog Technologies Ltd** Duolog Technologies, the Collaborative Design Automation™ Company, is an award-winning developer of groundbreaking EDA tools that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates chip integration platform employs a modular and extensible suite of tools for IO layer definition, IP packaging, connectivity and register management. The Socrates tools, built on the Eclipse platform and supporting the IP-XACT standard, shorten design cycles, reduce costs and greatly improve design quality through their Perfect-By-Construction™ methodology.  
[www.duolog.com](http://www.duolog.com)

**About Arteris** Arteris, Inc. provides Network-on-Chip (NoC) interconnect IP, NoC Generation and verification tools to improve performance of system-on-chip (SoC) architectures for multimedia, mobile, telecom, and other applications. Arteris' NoC solution allows chip developers to implement scalable, efficient and high-performance SoC designs, overcoming limitations of traditional layered or pipelined bus-based architectures. Results obtained by using Arteris NoC Solution include lower power, higher performance, lower risk of development and faster delivery of complex SoCs while increasing profits. Founded by networking experts, Arteris operates globally with headquarters in San Jose, California and an engineering center in Paris, France. Arteris is a private company backed by a group of international investors including TVM Capital, Crescendo Ventures, Ventech, Synopsys and DoCoMo Capital. More information can be found at <http://www.arteris.com>

**About IP-XACT** IP-XACT, a standard progressed by the SPIRIT consortium, defines a standard way for describing and handling multi-sourced IP components. This can enable automated design integration and configuration within multi-vendor design flows. The standardization effort in the SPIRIT consortium is driven by a coalition of leading semiconductor and EDA companies including Texas Instruments, ST, LSI, Freescale, NXP, Infineon, Cisco, Cadence, Synopsys and Mentor Graphics. Duolog is a contributing member of the Spirit consortium

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